

WHAT IS CLAIMED IS:

1. A method for modeling a circuit design comprising:
 - synthesizing a circuit design to create a first gate-level representation of the circuit design;
 - 5 analyzing a second gate-level representation of the circuit design to learn architecture information; and
 - resynthesizing the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design.
- 10 2. The method of Claim 1, wherein the second gate-level representation being created during a synthesis process.
3. The method of Claim 1, wherein the learned architecture information comprises logic network architecture in the second gate-level representation of the circuit design.
- 15 4. The method of Claim 1, wherein the analyzing comprises a resource sharing learning.
- 20 ^{SUB A1} 5. The method of Claim 4, wherein the resource sharing learning comprising:
 - creating one or more resource pairs from sharable resources in the first gate-level representation of the circuit design;
 - for each of the one or more resource pairs, synthesizing a subcircuit that shares the resource pair;
 - for each of the synthesized subcircuits, calculating a similarity with a corresponding subcircuit in the second gate-level representation of the circuit design;
 - 25 identifying the synthesized subcircuits having a high similarity with the corresponding subcircuit in the second gate-level representation of the circuit design; and
 - resynthesizing the first gate-level representation of the circuit design to include the subcircuits identified as having high similarity.
- 30 6. The method of Claim 1, wherein the analyzing comprises an operator order learning.

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7. The method of Claim 6, wherein the operator order learning comprising:
creating one or more operand pairs from operations in the first gate-level
representation of the circuit design;

for each of the one or more operand pairs, synthesizing a subcircuit for the
operand pair;

for each of the synthesized subcircuits, calculating a similarity with a
corresponding subcircuit in the second gate-level representation of the
circuit design;

identifying the synthesized subcircuits having a high similarity with the
corresponding subcircuit in the second gate-level representation of the circuit
design; and

resynthesizing the first gate-level representation of the circuit design to
include the subcircuits identified as having high similarity.

8. The method of Claim 7 further comprising, for each of the synthesized
subcircuits having high similarity, creating a new operand that signifies the output of the
operand pair associated with the synthesized subcircuit.

9. The method of Claim 1, wherein the analyzing comprises a
multiplier learning.

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10. The method of Claim 9, wherein the multiplier learning comprising:
identifying a multiplier in the first gate-level representation of the
circuit design;

identifying a corresponding multiplier subcircuit in the second gate-level
representation of the circuit design;

synthesizing the multiplier in the first gate-level representation with a
partial product generation implementation;

calculating a similarity for the synthesized partial product generation
subcircuit with the partial product generation subcircuit in the corresponding
multiplier in the second gate-level representation; and

resynthesizing the multiplier in the first gate-level representation to have
the partial product generation most similar to the partial product generation in the
second gate-level representation.

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11. The method of Claim 9, wherein the multiplier learning comprising:
analyzing a reduction tree structure in the second gate-level representation
of the circuit design; and
resynthesizing a reduction tree in the first gate-level representation from
the reduction tree structure learned from the second gate-level representation.

12. The method of Claim 1, wherein the analyzing comprises an operator
merging learning.

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13. The method of Claim 12, wherein the operator merging
learning comprising:

expressing a complex operation in the first gate-level representation as
a summation;

analyzing a reduction tree structure in the second gate-level representation
of the circuit design, the reduction tree corresponds to the complex operation; and

resynthesizing a reduction tree in the first gate-level representation from
the reduction tree structure learned from the second gate-level representation.

14. The method of Claim 1, wherein the analyzing comprising:
identifying a first subcircuit in the first gate-level representation of the
circuit design;

identifying a second subcircuit in the second gate-level representation of
the circuit design, the second subcircuit corresponding to the first subcircuit; and
calculating a similarity between the first subcircuit and the
second subcircuit.

15. The method of Claim 14, wherein calculating the similarity comprises
checking one or more circuit structures.

16. The method of Claim 14, wherein calculating the similarity comprises
checking one or more boolean functions.

17. The method of Claim 14, wherein calculating the similarity comprises
performing one or more simulations.

18. A computer-readable storage medium having stored thereon computer
instructions that, when executed by a computer, cause the computer to:

synthesize a circuit design to create a first gate-level representation of the
circuit design;

analyze a second gate-level representation of the circuit design to learn architecture information; and

resynthesize the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design.

19. The computer-readable storage medium of Claim 18, wherein the second gate-level representation being created during a synthesis process.

20. The computer-readable storage medium of Claim 18, wherein the learned architecture information comprises logic network architecture in the second gate-level representation of the circuit design.

21. The computer-readable storage medium of Claim 18, wherein the analyzing comprises a resource sharing learning.

22. The computer-readable storage medium of Claim 21, wherein the computer instructions that perform resource sharing learning further comprise computer instructions that, when executed by a computer, cause the computer to:

create one or more resource pairs from sharable resources in the first gate-level representation of the circuit design;

for each of the one or more resource pairs, synthesize a subcircuit that shares the resource pair;

for each of the synthesized subcircuits, calculate a similarity with a corresponding subcircuit in the second gate-level representation of the circuit design;

identify the synthesized subcircuits having a high similarity with the corresponding subcircuit in the second gate-level representation of the circuit design; and

resynthesize the first gate-level representation of the circuit design to include the subcircuits identified as having high similarity.

23. The computer-readable storage medium of Claim 18, wherein the analyzing comprises an operator order learning.

24. The computer-readable storage medium of Claim 23, wherein the computer instructions that perform operator order learning further comprise computer instructions that, when executed by a computer, cause the computer to:

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create one or more operand pairs from operations in the first gate-level representation of the circuit design;

for each of the one or more operand pairs, synthesize a subcircuit for the operand pair;

5 for each of the synthesized subcircuits, calculate a similarity with a corresponding subcircuit in the second gate-level representation of the circuit design;

identify the synthesized subcircuits having a high similarity with the corresponding subcircuit in the second gate-level representation of the circuit design; and

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resynthesize the first gate-level representation of the circuit design to include the subcircuits identified as having high similarity.

25. The computer-readable storage medium of Claim 24, wherein the computer instructions that perform operator order learning further comprise computer instructions that, when executed by a computer, cause the computer to, for each of the synthesized subcircuits having high similarity, create a new operand that signifies the output of the operand pair associated with the synthesized subcircuit.

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26. The computer-readable storage medium of Claim 18, wherein the analyzing comprises a multiplier learning.

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27. The computer-readable storage medium of Claim 26, wherein the computer instructions that perform multiplier learning further comprise computer instructions that, when executed by a computer, cause the computer to:

identify a multiplier in the first gate-level representation of the circuit design;

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identify a corresponding multiplier subcircuit in the second gate-level representation of the circuit design;

synthesize the multiplier in the first gate-level representation with a partial product generation implementation;

calculate a similarity for the synthesized partial product generation subcircuit with the partial product generation subcircuit in the corresponding multiplier in the second gate-level representation; and

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5 resynthesize the multiplier in the first gate-level representation to have the
partial product generation most similar to the partial product generation in the
second gate-level representation.

28. The computer-readable storage medium of Claim 26, wherein the
computer instructions that perform multiplier learning further comprise computer
instructions that, when executed by a computer, cause the computer to:

analyze a reduction tree structure in the second gate-level representation of
the circuit design; and

resynthesize a reduction tree in the first gate-level representation from the
reduction tree structure learned from the second gate-level representation.

29. The computer-readable storage medium of Claim 18, wherein the
analyzing comprises an operator merging learning.

30. The computer-readable storage medium of Claim 29, wherein the
computer instructions that perform operator merging learning further comprise computer
instructions that, when executed by a computer, cause the computer to:

express a complex operation in the first gate-level representation as
a summation;

analyze a reduction tree structure in the second gate-level representation of
the circuit design, the reduction tree corresponds to the complex operation; and

resynthesize a reduction tree in the first gate-level representation from the
reduction tree structure learned from the second gate-level representation.

31. The computer-readable storage medium of Claim 26, wherein the
computer instructions that perform analyzing further comprise computer instructions that,
when executed by a computer, cause the computer to:

identify a first subcircuit in the first gate-level representation of the
circuit design;

identify a second subcircuit in the second gate-level representation of the
circuit design, the second subcircuit corresponding to the first subcircuit; and

calculate a similarity between the first subcircuit and the second subcircuit.

32. The computer-readable storage medium of Claim 31, wherein calculating
the similarity comprises checking one or more circuit structures.

33. The computer-readable storage medium of Claim 31, wherein calculating
the similarity comprises checking one or more boolean functions.

34. The computer-readable storage medium of Claim 31, wherein calculating the similarity comprises performing one or more simulations.

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